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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/811,456	03/20/2001	Masahito Isoda	108075-00056	2125

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EXAMINER	
NGUYEN, LONG T	
ART UNIT	**PAPER NUMBER**
2816	

DATE MAILED: 10/17/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/811,456	ISODA, MASAHITO	
	Examiner	Art Unit	
	Long Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 August 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *19-53* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *19-30,33-35 and 38-49* is/are rejected.

7)☐ Claim(s) *31,32,36,37 and 50-53* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. *09/479,927* .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after allowance or after an Office action under *Ex Parte Quayle*, 25 USPQ 74, 453 O.G. 213 (Comm'r Pat. 1935). Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, prosecution in this application has been reopened pursuant to 37 CFR 1.114. Applicant's submission filed on 8/6/03 has been entered.

Response to Amendment

2. The amendment filed on 8/6/03 has been entered in the case.

3. In this office action, the allowable subject matter in the last office action has been withdrawn based on the following rejection set forth below.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 23, 26, 29, 34, 48 and 49 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

With respect to claim 23, "a predetermined voltage" on the last 2 lines of the claim is unclear antecedent basis, i.e., it is not clear whether it is the same as the predetermined voltage recited earlier in the claim (last line of claim 22). Note that the similar problem also exists in claims 26, 29, and 34.

With respect to claims 48 and 49, the recitation "wherein each of the first and second circuits includes only on input terminal and only one output terminal" is indefinite because it is misdescriptive since it is inconsistent with what is disclosed and shown. Figure 5 of the drawings shows that the first circuit (13) and the second circuit (14) having more than one input terminal (circuit 13 in Figure 5 having input terminals Z, S and S/; and circuit 14 in Figure 5 having input terminals IN, S, and S/). Also, in Figure 2 of the drawings, the second circuit (Tp3, Tp4, 6, 7) including more than one input terminal (terminals IN and S/), and the first circuit (Tn5) having input terminals Z and S/. Note that the terminals receiving the enable signals are also considered as the input terminals (i.e., input enable terminals). Insofar as understood, the disclosure only disclosed and shown that each of the first and second circuits including only one output terminal.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. Claims 19-30, 33-36 and 38-49 are rejected under 35 U.S.C. 102(b) as being anticipated by Fischer et al. (USP 5,889,419).

With respect to claim 19, Figure 3 of the Fischer et al. reference discloses a circuit, which includes: a differential amplifier circuit (302), disposed between a first power supply and a

second power supply (inherently between the power supply Vdd and ground), for receiving first and second input signals (P, N) and generating an amplifier signal (output of 302) corresponding to a voltage difference between the first and second input signals (P, N); a first circuit (M3, M4), coupled to the differential amplifier circuit (302), for receiving the amplified signal from the differential amplifier circuit (302); a second circuit (301), disposed between the first power supply and second power supply (inherently between the power supply Vdd and ground), for receiving the first input signal (P); and a control circuit (306) for selectively enabling one of the differential amplifier circuit (302) and the second circuit (301) in accordance with a control signal (signal at node 315) while isolating the other one of the differential amplifier circuit and the second circuit from at least one of the first and the second power supply (Col. 2, lines 48-59).

With respect to claim 20, the circuit in Figure 3 of the Fischer et al. reference meets the limitation that the control circuit (306) enables the differential amplifier circuit (302) and disable the second circuit (301) when the first and second input signals (P, N) have amplitudes smaller than a predetermined voltage (see lines 45-52 of Col. 1 and lines 5-65 of Col. 2).

With respect to claim 21, the circuit in Figure 3 of the Fischer et al. reference meets the limitation that the control circuit (306) disables the differential amplifier circuit (302) and enables the second circuit (301) when the first and second input signals (P, N) have amplitudes greater than a predetermined voltage (see lines 45-52 of Col. 1 and lines 5-65 of Col. 2).

With respect to claims 22 and 23, these claims are rejected for the same reasons as in claims 20 and 21, respectively.

With respect to claim 24, it is seen in the Fischer et al. reference that the differential amplifier (302) including a constant current source, and wherein the control circuit (306) disables

the differential amplifier (302) by stopping a current from flowing through the constant current source (see line 48 of Col. 2 to line 15 of Col. 3).

With respect to claim 25, this claim is rejected for the same reasons as in claim 21.

With respect to claim 26, this claim is rejected for the same reasons as in claim 20.

With respect to claim 27, this claim is rejected for the same reasons as in claim 24.

With respect to claim 28, Figure 3 of the Fischer et al. reference discloses a circuit, which includes: a differential amplifier circuit (302), disposed between a first power supply and a second power supply (inherently between the power supply Vdd and ground), for receiving first and second input signals (P, N) and generating an amplifier signal (output of 302) corresponding to a voltage difference between the first and second input signals (P, N); a first circuit (M3, M4), coupled to the differential amplifier circuit (302), for receiving the amplified signal from the differential amplifier circuit (302); a second circuit (301), disposed between the first power supply and second power supply (inherently between the power supply Vdd and ground), for receiving the first input signal (P); and a control circuit (306) for selectively enabling one of the differential amplifier circuit (302) and the first circuit (M3, M4), and the second circuit (301) in accordance with a control signal (signal at node 315), wherein the differential amplifier circuit (302) and the first circuit (M3, M4) are enabled and the second circuit (301) is disabled when the first and second input signals (P, N) have amplitudes smaller than a predetermined voltage (see lines 45-52 of Col. 1 and lines 5-65 of Col. 2).

With respect to claim 29, it is seen in the operation of Figure 3 of the Fischer et al. reference that the differential amplifier circuit (302) and the first circuit (M3, M4) are disabled and the second circuit (301) is enabled when the first and second input signals (P, N) have

amplitudes greater than a predetermined voltage (see lines 45-52 of Col. 1 and lines 5-65 of Col. 2).

With respect to claim 30, Figure 3 shows the circuit including a driver circuit (the two inverter connected in series providing the output Z) connected to the first and second circuits, for receiving an output signal from the enabled one of the first and second circuits enabled by the control circuit.

With respect to claims 33-35, these claims are rejected for the same reasons as in claims 29, 28 and 30, respectively.

With respect to claims 38-47, these claims are rejected for the same manners as discussed above.

Insofar as understood in claims 48 and 49, Figure 3 shows that each of the first (M3, M4) and second (301) circuits including only one output terminal.

Allowable Subject Matter

8. Claims 31, 32, 36, 37 and 50-53 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 31, 32, 36 and 37 would be allowed because the prior art of record fails to disclose or suggest that, in combination with other limitations, each of the first and second circuits including an inverter, a PMOS transistor, and an NMOS transistor with the recited connections and operations set forth therein.

Claims 50 and 52 would be allowed because the prior art of record fails to disclose or suggest that, in combination with other limitations, the first circuit and the second circuit including an inverter and a PMOS transistor with the recited connections set forth therein.

Claims 51 and 53 would be allowed because the prior art of record fails to disclose or suggest that, in combination with other limitations, the first circuit and the second circuit including an inverter and an NMOS transistor with the recited connections set forth therein.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directly to Examiner Long Nguyen whose telephone number is (703) 308-6063. The Examiner can normally be reached on Monday to Friday from 8:30am to 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan, can be reached at (703) 308-4876. The fax number for this group is (703) 872-9306.

Any inquiry of general nature or relating to the status of this application or proceeding should be directed to the group receptionist whose telephone number is (703) 308-0956.

LN
Date: October 9, 2003

Long Nguyen
Art Unit: 2816